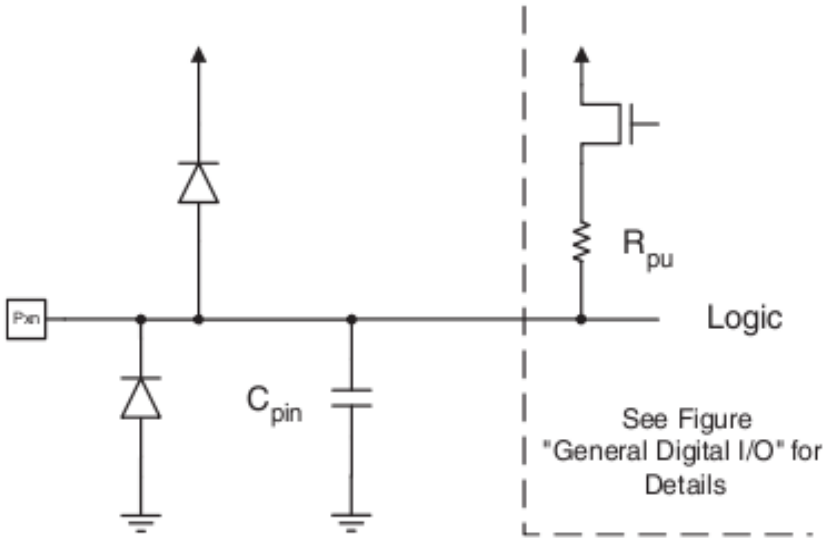
11. I/O-Ports

11.1 Introduction

All AVR ports have true Read-Modify-Write functionality when used as general digital I/O ports. This means that the direction of one port pin can be changed without unintentionally changing the direction of any other pin with the SBI and CBI instructions. The same applies when changing drive value (if configured as output) or enabling/disabling of pull-up resistors (if configured as input). Each output buffer has symmetrical drive characteristics with both high sink and source capability. The pin driver is strong enough to drive LED displays directly. All port pins have individually selectable pull-up resistors with a supply-voltage invariant resistance. All I/O pins have protection diodes to both V_{CC} and Ground as indicated in Figure 11-1. Refer to "Electrical Characteristics" on page 262 for a complete list of parameters.

Figure 11-1. I/O Pin Equivalent Schematic



All registers and bit references in this section are written in general form. A lower case "x" represents the numbering letter for the port, and a lower case "n" represents the bit number. However, when using the register or bit defines in a program, the precise form must be used. For example, PORTB3 for bit no. 3 in Port B, here documented generally as PORTxn. The physical I/O Registers and bit locations are listed in "Register Description for I/O-Ports" on page 82.

Three I/O memory address locations are allocated for each port, one each for the Data Register – PORTx, Data Direction Register – DDRx, and the Port Input Pins – PINx. The Port Input Pins I/O location is read only, while the Data Register and the Data Direction Register are read/write. However, writing a logic one to a bit in the PINx Register, will result in a toggle in the corresponding bit in the Data Register. In addition, the Pull-up Disable – PUD bit in MCUCR disables the pull-up function for all pins in all ports when set.

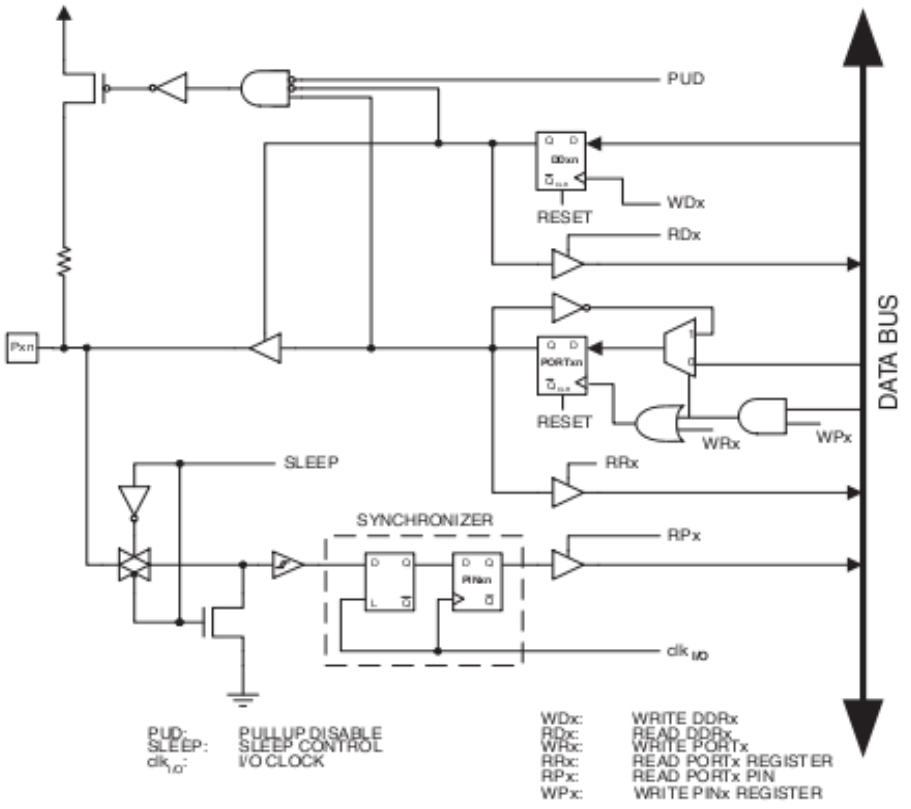
Using the I/O port as General Digital I/O is described in "Ports as General Digital I/O" on page 68. Most port pins are multiplexed with alternate functions for the peripheral features on the device. How each alternate function interferes with the port pin is described in "Alternate Port Functions" on page 72. Refer to the individual module sections for a full description of the alternate functions.

Note that enabling the alternate function of some of the port pins does not affect the use of the other pins in the port as general digital I/O.

11.2 Ports as General Digital I/O

The ports are bi-directional I/O ports with optional internal pull-ups. Figure 11-2 shows a functional description of one I/O-port pin, here generically called Pxn.

Figure 11-2. General Digital I/O[1]



Note: 1. WRx, WPx, WDx, RRx, RPx, and RDx are common to all pins within the same port. $clk_{I/O}$, SLEEP, and PUD are common to all ports.

11.2.1 Configuring the Pin

Each port pin consists of three register bits: DDxn, PORTxn, and PINxn. As shown in "Register Description for I/O-Ports" on page 82, the DDxn bits are accessed at the DDRx I/O address, the PORTxn bits at the PORTx I/O address, and the PINxn bits at the PINx I/O address.

The DDxn bit in the DDRx Register selects the direction of this pin. If DDxn is written logic one, Pxn is configured as an output pin. If DDxn is written logic zero, Pxn is configured as an input pin.

If PORTxn is written logic one when the pin is configured as an input pin, the pull-up resistor is activated. To switch the pull-up resistor off, PORTxn has to be written logic zero or the pin has to be configured as an output pin. The port pins are tri-stated when reset condition becomes active, even if no clocks are running.

If PORTxn is written logic one when the pin is configured as an output pin, the port pin is driven high (one). If PORTxn is written logic zero when the pin is configured as an output pin, the port pin is driven low (zero).

11.2.2 Toggling the Pin

Writing a logic one to PINxn toggles the value of PORTxn, independent on the value of DDRxn. Note that the SBI instruction can be used to toggle one single bit in a port.

11.2.3 Switching Between Input and Output

When switching between tri-state ({DDxn, PORTxn} = 0b00) and output high ({DDxn, PORTxn} = 0b11), an intermediate state with either pull-up enabled {DDxn, PORTxn} = 0b01) or output low ({DDxn, PORTxn} = 0b10) occurs. Normally, the pull-up enabled state is fully acceptable, as a high-impedant environment will not notice the difference between a strong high driver and a pull-up. If this is not the case, the PUD bit in the MCUCR Register can be set to disable all pull-ups in all ports.

Switching between input with pull-up and output low generates the same problem. The user must use either the tri-state ({DDxn, PORTxn} = 0b00) or the output high state ({DDxn, PORTxn} = 0b11) as an intermediate step.

Table 11-1 summarizes the control signals for the pin value.

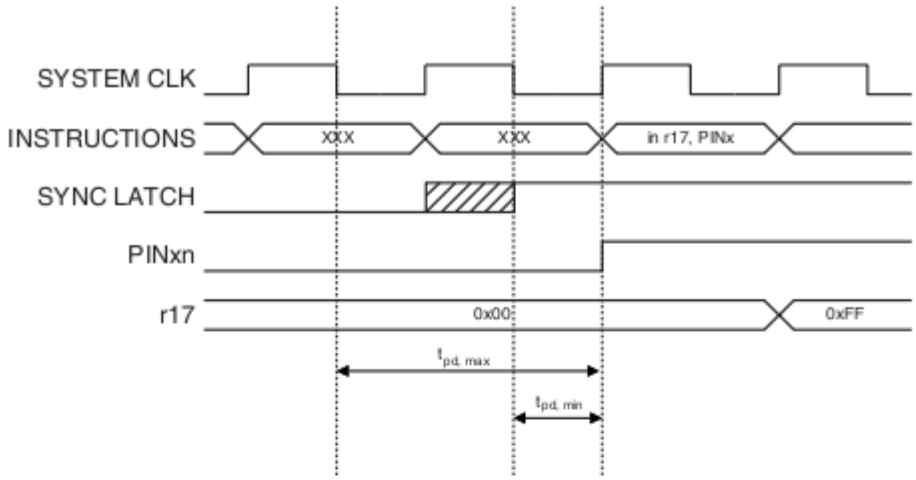
Table 11-1. Port Pin Configurations

DDxn	PORTxn	PUD (in MCUCR)	I/O	Pull-up	Comment
0	0	X	Input	No	Tri-state (Hi-Z)
0	1	0	Input	Yes	Pxn will source current if ext. pulled low.
0	1	1	Input	No	Tri-state (Hi-Z)
1	0	X	Output	No	Output Low (Sink)
1	1	X	Output	No	Output High (Source)

11.2.4 Reading the Pin Value

Independent of the setting of Data Direction bit DDxn, the port pin can be read through the PINxn Register bit. As shown in Figure 11-2, the PINxn Register bit and the preceding latch constitute a synchronizer. This is needed to avoid metastability if the physical pin changes value near the edge of the internal clock, but it also introduces a delay. Figure 11-3 shows a timing diagram of the synchronization when reading an externally applied pin value. The maximum and minimum propagation delays are denoted $t_{pd,max}$ and $t_{pd,min}$ respectively.

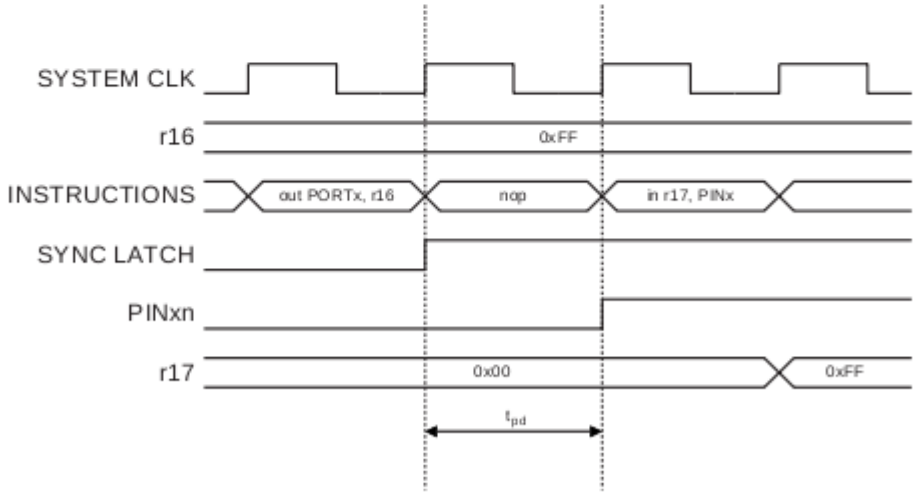
Figure 11-3. Synchronization when Reading an Externally Applied Pin value



Consider the clock period starting shortly after the first falling edge of the system clock. The latch is closed when the clock is low, and goes transparent when the clock is high, as indicated by the shaded region of the “SYNC LATCH” signal. The signal value is latched when the system clock goes low. It is clocked into the PINxn Register at the succeeding positive clock edge. As indicated by the two arrows tpd,max and tpd,min, a single signal transition on the pin will be delayed between ½ and 1½ system clock period depending upon the time of assertion.

When reading back a software assigned pin value, a nop instruction must be inserted as indicated in Figure 11-4. The out instruction sets the “SYNC LATCH” signal at the positive edge of the clock. In this case, the delay tpd through the synchronizer is 1 system clock period.

Figure 11-4. Synchronization when Reading a Software Assigned Pin Value



The following code example shows how to set port B pins 0 and 1 high, 2 and 3 low, and define the port pins from 4 to 7 as input with pull-ups assigned to port pins 6 and 7. The resulting pin values are read back again, but as previously discussed, a *nop* instruction is included to be able to read back the value recently assigned to some of the pins.

Assembly Code Example[1]

```
...
; Define pull-ups and set outputs high
; Define directions for port pins
ldi   r16,(1<<PB7)|(1<<PB6)|(1<<PB1)|(1<<PB0)
ldi   r17,(1<<DDB3)|(1<<DDB2)|(1<<DDB1)|(1<<DDB0)
out   PORTB,r16
out   DDRB,r17
; Insert nop for synchronization
nop
; Read port pins
in    r16,PINB
...
```

C Code Example

```
unsigned char i;
...
/* Define pull-ups and set outputs high */
/* Define directions for port pins */
PORTB = (1<<PB7)|(1<<PB6)|(1<<PB1)|(1<<PB0);
DDRB = (1<<DDB3)|(1<<DDB2)|(1<<DDB1)|(1<<DDB0);
/* Insert nop for synchronization*/
__no_operation();
/* Read port pins */
i = PINB;
...
```

Note: 1. For the assembly program, two temporary registers are used to minimize the time from pull-ups are set on pins 0, 1, 6, and 7, until the direction bits are correctly set, defining bit 2 and 3 as low and redefining bits 0 and 1 as strong high drivers.

11.2.5 Digital Input Enable and Sleep Modes

As shown in Figure 11-2, the digital input signal can be clamped to ground at the input of the schmitt-trigger. The signal denoted SLEEP in the figure, is set by the MCU Sleep Controller in Power-down mode, Power-save mode, and Standby mode to avoid high power consumption if some input signals are left floating, or have an analog signal level close to $V_{CC}/2$.

SLEEP is overridden for port pins enabled as external interrupt pins. If the external interrupt request is not enabled, SLEEP is active also for these pins. SLEEP is also overridden by various other alternate functions as described in "Alternate Port Functions" on page 72.

If a logic high level ("one") is present on an asynchronous external interrupt pin configured as "Interrupt on Rising Edge, Falling Edge, or Any Logic Change on Pin" while the external interrupt is *not* enabled, the corresponding External Interrupt Flag will be set when resuming from the above mentioned Sleep mode, as the clamping in these sleep mode produces the requested logic change.

11.2.6 Unconnected Pins

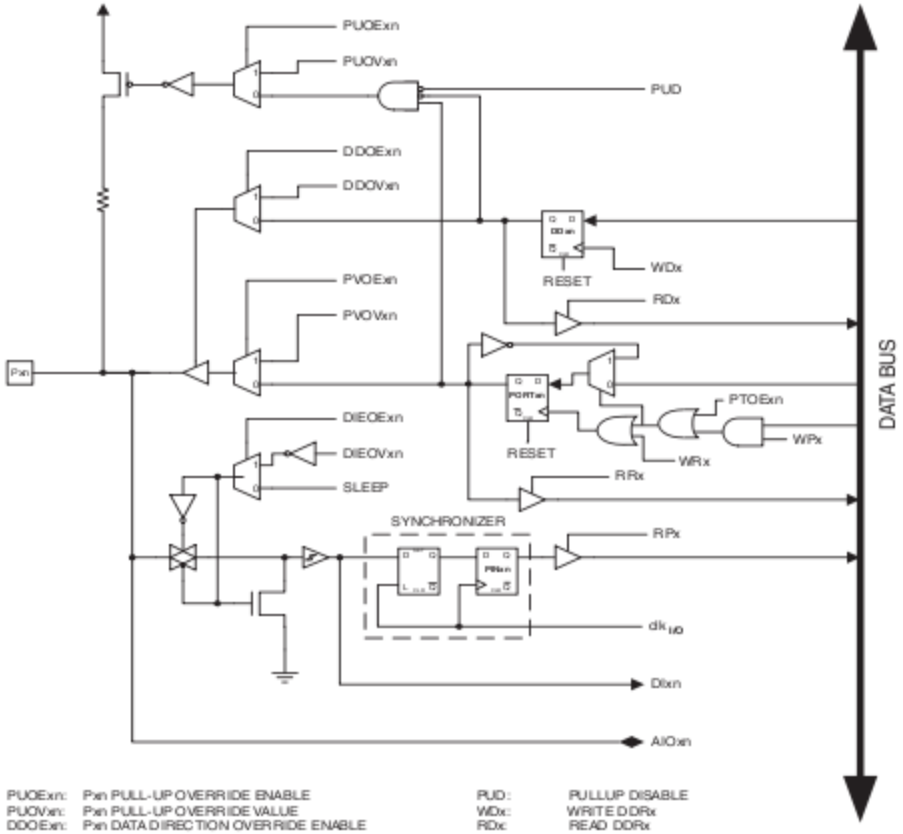
If some pins are unused, it is recommended to ensure that these pins have a defined level. Even though most of the digital inputs are disabled in the deep sleep modes as described above, floating inputs should be avoided to reduce current consumption in all other modes where the digital inputs are enabled (Reset, Active mode and Idle mode).

The simplest method to ensure a defined level of an unused pin, is to enable the internal pull-up. In this case, the pull-up will be disabled during reset. If low power consumption during reset is important, it is recommended to use an external pull-up or pull-down. Connecting unused pins directly to V_{CC} or GND is not recommended, since this may cause excessive currents if the pin is accidentally configured as an output.

11.3 Alternate Port Functions

Most port pins have alternate functions in addition to being general digital I/Os. Figure 11-5 shows how the port pin control signals from the simplified Figure 11-2 can be overridden by alternate functions. The overriding signals may not be present in all port pins, but the figure serves as a generic description applicable to all port pins in the AVR microcontroller family.

Figure 11-5. Alternate Port Functions[1]



PUOExn:	Pxn PULL-UP OVERRIDE ENABLE	PUD:	PULLUP DISABLE
PUOVxn:	Pxn PULL-UP OVERRIDE VALUE	WDx:	WRITE DDRx
DDOExn:	Pxn DATA DIRECTION OVERRIDE ENABLE	RDx:	READ DDRx
DDOVxn:	Pxn DATA DIRECTION OVERRIDE VALUE	RRx:	READ PORTx REGISTER
PVOExn:	Pxn PORT VALUE OVERRIDE ENABLE	WRx:	WRITE PORTx
PVOVxn:	Pxn PORT VALUE OVERRIDE VALUE	RPx:	READ PORTx PIN
DIEOExn:	Pxn DIGITAL INPUT-ENABLE OVERRIDE ENABLE	WPx:	WRITE PINx
DIEOVxn:	Pxn DIGITAL INPUT-ENABLE OVERRIDE VALUE	$clk_{I/O}$:	I/O CLOCK
SLEEP:	SLEEP CONTROL	DIxn:	DIGITAL INPUT PIN n ON PORTx
PTOExn:	Pxn, PORT TOGGLE OVERRIDE ENABLE	AIOxn:	ANALOG INPUT/OUTPUT PIN n ON PORTx

Note: 1. WRx, WPx, WDx, RRx, RPx, and RDx are common to all pins within the same port. $clk_{I/O}$, SLEEP, and PUD are common to all ports. All other signals are unique for each pin.

Table 11-2 summarizes the function of the overriding signals. The pin and port indexes from Figure 11-5 are not shown in the succeeding tables. The overriding signals are generated internally in the modules having the alternate function.

Table 11-2. Generic Description of Overriding Signals for Alternate Functions

Signal Name	Full Name	Description
PUOE	Pull-up Override Enable	If this signal is set, the pull-up enable is controlled by the PUOV signal. If this signal is cleared, the pull-up is enabled when {DDxn, PORTxn, PUD} = 0b010.
PUOV	Pull-up Override Value	If PUOE is set, the pull-up is enabled/disabled when PUOV is set/cleared, regardless of the setting of the DDxn, PORTxn, and PUD Register bits.
DDOE	Data Direction Override Enable	If this signal is set, the Output Driver Enable is controlled by the DDOV signal. If this signal is cleared, the Output driver is enabled by the DDxn Register bit.
DDOV	Data Direction Override Value	If DDOE is set, the Output Driver is enabled/disabled when DDOV is set/cleared, regardless of the setting of the DDxn Register bit.
PVOE	Port Value Override Enable	If this signal is set and the Output Driver is enabled, the port value is controlled by the PVOV signal. If PVOE is cleared, and the Output Driver is enabled, the port Value is controlled by the PORTxn Register bit.
PVOV	Port Value Override Value	If PVOE is set, the port value is set to PVOV, regardless of the setting of the PORTxn Register bit.
PTOE	Port Toggle Override Enable	If PTOE is set, the PORTxn Register bit is inverted.
DIEOE	Digital Input Enable Override Enable	If this bit is set, the Digital Input Enable is controlled by the DIEOV signal. If this signal is cleared, the Digital Input Enable is determined by MCU state (Normal mode, sleep mode).
DIEOV	Digital Input Enable Override Value	If DIEOE is set, the Digital Input is enabled/disabled when DIEOV is set/cleared, regardless of the MCU state (Normal mode, sleep mode).
DI	Digital Input	This is the Digital Input to alternate functions. In the figure, the signal is connected to the output of the schmitt trigger but before the synchronizer. Unless the Digital Input is used as a clock source, the module with the alternate function will use its own synchronizer.
AIO	Analog Input/Output	This is the Analog Input/output to/from alternate functions. The signal is connected directly to the pad, and can be used bi-directionally.

The following subsections shortly describe the alternate functions for each port, and relate the overriding signals to the alternate function. Refer to the alternate function description for further details.

11.3.1 MCU Control Register – MCUCR

Bit	7	6	5	4	3	2	1	0	
	JTD	–	–	PUD	–	–	IVSEL	IVCE	MCUCR

Read/Write	R/W	R	R	R/W	R	R	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

- **Bit 4 – PUD: Pull-up Disable**

When this bit is written to one, the pull-ups in the I/O ports are disabled even if the DDxn and PORTxn Registers are configured to enable the pull-ups ({DDxn, PORTxn} = 0b01). See "Configuring the Pin" on page 68 for more details about this feature.

11.3.2 Alternate Functions of Port B

The Port B pins with alternate functions are shown in Table 11-3.

Table 11-3. Port B Pins Alternate Functions

Port Pin	Alternate Functions
PB7	OC0A/OC1C/PCINT7 (Output Compare and PWM Output A for Timer/Counter0, Output Compare and PWM Output C for Timer/Counter1 or Pin Change Interrupt 7)
PB6	PCINT6 (Pin Change Interrupt 6)
PB5	PCINT5 (Pin Change Interrupt 5)
PB4	T1/PCINT4 (Timer/Counter1 Clock Input or Pin Change Interrupt 4)
PB3	PDO/MISO/PCINT3 (Programming Data Output or SPI Bus Master Input/Slave Output or Pin Change Interrupt 3)
PB2	PDI/MOSI/PCINT2 (Programming Data Input or SPI Bus Master Output/Slave Input or Pin Change Interrupt 2)
PB1	SCLK/PCINT1 (SPI Bus Serial Clock or Pin Change Interrupt 1)
PB0	$\overline{SS}$/PCINT0 (SPI Slave Select input or Pin Change Interrupt 0)

The alternate pin configuration is as follows:

- **OC0A/OC1C/PCINT7, Bit 7**

OC0A, Output Compare Match A output: The PB7 pin can serve as an external output for the Timer/Counter0 Output Compare. The pin has to be configured as an output (DDB7 set "one") to serve this function. The OC0A pin is also the output pin for the PWM mode timer function.

OC1C, Output Compare Match C output: The PB7 pin can serve as an external output for the Timer/Counter1 Output Compare C. The pin has to be configured as an output (DDB7 set "one") to serve this function. The OC1C pin is also the output pin for the PWM mode timer function.

PCINT7, Pin Change Interrupt source 7: The PB7 pin can serve as an external interrupt source.

- **PCINT6, Bit 6**

PCINT6, Pin Change Interrupt source 6: The PB6 pin can serve as an external interrupt source.

- **PCINT5, Bit 5**

PCINT5, Pin Change Interrupt source 5: The PB5 pin can serve as an external interrupt source.

- **T1/PCINT4, Bit 4**

T1, Timer/Counter1 counter source.

PCINT4, Pin Change Interrupt source 4: The PB4 pin can serve as an external interrupt source.

- **PDO/MISO/PCINT3 – Port B, Bit 3**

PDO, SPI Serial Programming Data Output. During Serial Program Downloading, this pin is used as data output line for the AT90USB82/162.

MISO: Master Data input, Slave Data output pin for SPI channel. When the SPI is enabled as a master, this pin is configured as an input regardless of the setting of DDB3. When the SPI is enabled as a slave, the data direction of this pin is controlled by DDB3. When the pin is forced to be an input, the pull-up can still be controlled by the PORTB3 bit.

PCINT3, Pin Change Interrupt source 3: The PB3 pin can serve as an external interrupt source.

- **PDI/MOSI/PCINT2 – Port B, Bit 2**

PDI, SPI Serial Programming Data Input. During Serial Program Downloading, this pin is used as data input line for the AT90USB82/162.

MOSI: SPI Master Data output, Slave Data input for SPI channel. When the SPI is enabled as a slave, this pin is configured as an input regardless of the setting of DDB2. When the SPI is enabled as a master, the data direction of this pin is controlled by DDB2. When the pin is forced to be an input, the pull-up can still be controlled by the PORTB2 bit.

PCINT2, Pin Change Interrupt source 2: The PB2 pin can serve as an external interrupt source.

- **SCK/PCINT1 – Port B, Bit 1**

SCK: Master Clock output, Slave Clock input pin for SPI channel. When the SPI is enabled as a slave, this pin is configured as an input regardless of the setting of DDB1. When the SPI0 is enabled as a master, the data direction of this pin is controlled by DDB1. When the pin is forced to be an input, the pull-up can still be controlled by the PORTB1 bit. This pin also serves as Clock for the Serial Programming interface.

PCINT1, Pin Change Interrupt source 1: The PB1 pin can serve as an external interrupt source.

- **$\overline{SS}$/PCINT0 – Port B, Bit 0**

$\overline{SS}$: Slave Port Select input. When the SPI is enabled as a slave, this pin is configured as an input regardless of the setting of DDB0. As a slave, the SPI is activated when this pin is driven low. When the SPI is enabled as a master, the data direction of this pin is controlled by DDB0. When the pin is forced to be an input, the pull-up can still be controlled by the PORTB0 bit.

PCINT0, Pin Change Interrupt source 0: The PB0 pin can serve as an external interrupt source.

Table 11-4 and Table 11-5 relate the alternate functions of Port B to the overriding signals shown in Figure 11-5 on page 72. SPI MSTR INPUT and SPI SLAVE OUTPUT constitute the MISO signal, while MOSI is divided into SPI MSTR OUTPUT and SPI SLAVE INPUT.

PCINT0, Pin Change Interrupt source 0: The PB0 pin can serve as an external interrupt source

.Table 11-4 and Table 11-5 relate the alternate functions of Port B to the overriding signals shown in Figure 11-5 on page 72. SPI MSTR INPUT and SPI SLAVE OUTPUT constitute the MISO signal, while MOSI is divided into SPI MSTR OUTPUT and SPI SLAVE INPUT..

Table 11-4. Overriding Signals for Alternate Functions in PB7..PB4

Signal Name	PB7/OC0A/OC1C/PCINT7	PB6/PCINT6	PB5/PCINT5	PB4/T1/PCINT4
PUOE	0	0	0	0
PUOV	0	0	0	0
DDOE	0	0	0	0
DDOV	0	0	0	0
PVOE	OC0A/OC1C ENABLE	0	0	0
PVOV	OC0A/OC1C	0	0	0
DIEOE	PCINT7 • PCIE0	PCINT6 • PCIE0	PCINT5 • PCIE0	PCINT4 • PCIE0
DIEOV	1	1	1	1
DI	PCINT7 INPUT	PCINT6 INPUT	PCINT5 INPUT	PCINT4 INPUT T1 INPUT
AIO	–	–	–	–

Table 11-5. Overriding Signals for Alternate Functions in PB3..PB0

Signal Name	PB3/MISO/PCINT3/PDO	PB2/MOSI/PCINT2/PDI	PB1/SCK/PCINT1	PB0/$\overline{SS}$/PCINT0
PUOE	SPE • MSTR	SPE • $\overline{MSTR}$	SPE • $\overline{MSTR}$	SPE • $\overline{MSTR}$
PUOV	PORTB3 • $\overline{PUD}$	PORTB2 • $\overline{PUD}$	PORTB1 • $\overline{PUD}$	PORTB0 • $\overline{PUD}$
DDOE	SPE • MSTR	SPE • $\overline{MSTR}$	SPE • $\overline{MSTR}$	SPE • $\overline{MSTR}$
DDOV	0	0	0	0
PVOE	SPE • $\overline{MSTR}$	SPE • MSTR	SPE • MSTR	0
PVOV	SPI SLAVE OUTPUT	SPI MSTR OUTPUT	SCK OUTPUT	0
DIEOE	PCINT3 • PCIE0	PCINT2 • PCIE0	PCINT1 • PCIE0	PCINT0 • PCIE0
DIEOV	1	1	1	1
DI	SPI MSTR INPUT PCINT3 INPUT	SPI SLAVE INPUT PCINT2 INPUT	SCK INPUT PCINT1 INPUT	SPI $\overline{SS}$ PCINT0 INPUT
AIO	–	–	–	–

11.3.3 Alternate Functions of Port C

The Port C alternate function is as follows:

Table 11-6. Port C Pins Alternate Functions

Port Pin	Alternate Function
PC7	ICP1/INT4/CLKO
PC6	PCINT8/OC1A
PC5	PCINT9/OC1B
PC4	PCINT10
-	-
PC2	PCINT11
PC1	Reset, dW
PC0	XTAL2

The alternate pin configuration is as follows:

- **ICP1/INT4/CLK0, Bit 7**

ICP1, Input Capture pin 1 :The PC7 pin can act as an input capture for Timer/Counter1.

INT4, External Interrupt source 4 : The PC7 pin can serve as an external interrupt source to the MCU.

CLK0, Clock Output : The PC7 pin can serve as oscillator clock ouput if the feature is enabled by fuse.

- **PCINT8/OC1A, Bit 6**

PCINT8, Pin Change Interrupt source 8 : The PC6 pin can serve as an external interrupt source.

OC1A, Output Compare Match A output: The PC6 pin can serve as an external output for the Timer/Counter1 Output Compare. The pin has to be configured as an output (DDC6 set “one”) to serve this function. The OC1A pin is also the output pin for the PWM mode timer function.

- **PCINT9/OC1B, Bit 5**

PCINT9, Pin Change Interrupt source 9: The PC5 pin can serve as an external interrupt source.

OC1B, Output Compare Match B output: The PC5 pin can serve as an external output for the Timer/Counter1 Output Compare. The pin has to be configured as an output (DDC5 set “one”) to serve this function. The OC1B pin is also the output pin for the PWM mode timer function.

- **PCINT10, Bit 4**

PCINT10, Pin Change Interrupt source 10 : The PC4 pin can serve as an external interrupt source.

- **PCINT11, Bit 2**

PCINT11, Pin Change Interrupt source 11 : The PC2 pin can serve as an external interrupt source.

- **Reset/dW, Bit 1**

Reset, Reset input. External Reset input is active low and enabled by unprogramming ("1") the RSTDISBL Fuse. Pullup is activated and output driver and digital input are deactivated when the pin is used as the RESET pin.

dW, debugWire channel. When the debugWIRE Enable (DWEN) Fuse is programmed and Lock bits are unprogrammed, the debugWIRE system within the target device is activated. The RESET port pin is configured as a wired -AND (open-drain) bi-directional I/O pin with pull-up enabled and becomes the communication gateway between the target and the emulator.

- **XTAL2, Bit 0**

XTAL2, Oscillator. The PC0 pin can serve as Inverting Output for internal Oscillator amplifier.

Table 11-7 and Table 11-8 relate the alternate functions of Port C to the overriding signals shown in Figure 11-5 on page 72.

Table 11-7. Overriding Signals for Alternate Functions in PC7..PC4

Signal Name	PC7/ICP1/INT4/CLK0	PC6/PCINT8/OC1A	PC5/PCINT9/OC1B	PC4/PCINT10
PUOE	0	0	0	0
PUOV	0	0	0	0
DDOE	0	0	0	0
DDOV	0	0	0	0
PVOE	0	OC1A ENABLE	OC1B ENABLE	0
PVOV	0	OC1A	OC1B	0
DIEOE	INT4 ENABLE	PCINT8 ENABLE	PCINT9 ENABLE	PCINT10 ENABLE
DIEOV	1	1	1	1
DI	INT4 INPUT	PCINT8 INPUT	PCINT9 INPUT	PCINT10 INPUT
AIO	–	–	–	–

Table 11-8. Overriding Signals for Alternate Functions in PC2..PC0

Signal Name	PC2/PCINT11	PC1/$\overline{\text{RESET}}$/dW	PC0/XTAL2
PUOE	0	0	0
PUOV	0	0	0
DDOE	0	0	0
DDOV	0	0	0
PVOE	0	0	0
PVOV	0	0	0
DIEOE	PCINT11 ENABLE	0	0
DIEOV	1	0	0
DI	PCINT11 INPUT	–	–
AIO	–	–	–

11.3.4 Alternate Functions of Port D

The Port D pins with alternate functions are shown in Table 11-9.

Table 11-9. Port D Pins Alternate Functions

Port Pin	Alternate Function
PD7	$\overline{\text{HWB}}$/TO/INT7/$\overline{\text{CTS}}$
PD6	INT6/$\overline{\text{RTS}}$
PD5	XCK1/PCINT12 (USART1 External Clock Input/Output)
PD4	INT5
PD3	$\overline{\text{INT3}}$/TXD1 (External Interrupt3 Input or USART1 Transmit Pin)
PD2	$\overline{\text{INT2}}$/AIN1/RXD1(External Interrupt2 Input or USART1 Receive Pin)
PD1	$\overline{\text{INT1}}$/AIN0 (External Interrupt1 Input)
PD0	$\overline{\text{INT0}}$/OC0B (External Interrupt0 Input)

The alternate pin configuration is as follows:

- **$\overline{\text{HWB}}$/TO/INT7/$\overline{\text{CTS}}$, Bit 7**

$\overline{\text{HWB}}$, Hardware Boot : The PD7 pin can serve as

TO, Timer/Counter0 counter source.

INT7, External Interrupt source 7: The PD7 pin can serve as an external interrupt source to the MCU.

$\overline{\text{CTS}}$, USART1 Transmitter Flow Control. This pin can control the transmitter in function of its state.

- **INT6/$\overline{\text{RTS}}$,Bit 6**

INT6, External Interrupt source 6: The PD6 pin can serve as an external interrupt source to the MCU.

$\overline{\text{RTS}}$, USART1 Receiver Flow Control. This pin can control the receiver in function of its state.

- **XCK1/PCINT12, Bit 5**

XCK1, USART1 External Clock : The data direction register DDRD5 controls whether the clock is output (DDRD5 set) or input (DDRD5 cleared). The XCK1 pin is active only when the USART1 operates in Synchronous Mode.

PCINT12, Pin Change Interrupt source 12: The PD5 pin can serve as an external interrupt source.

- **INT5, Bit 4**

INT5, External Interrupt source 5: The PD4 pin can serve as an external interrupt source to the MCU.

- **$\overline{\text{INT3}}$/TXD1, Bit 3**

INT3, External Interrupt source 3: The PD3 pin can serve as an external interrupt source to the MCU.

TXD1, USART1 Transmit Data : When the USART1 Transmitter is enabled, this pin is configured as an ouput regardless of DDRD3.

- **$\overline{\text{INT2}}$/AIN1/RXD1, Bit 2**

INT2, External Interrupt source 2: The PD2 pin can serve as an external interrupt source to the MCU.

AIN1, Analog Comparator Negative input. This pin is directly connected to the negative input of the Analog Comparator.

RXD1, USART1 Receive Data : When the USART1 Receiver is enabled, this pin is configured as an input regardless of DDRD2. When the USART forces this pin to be an input, the pull-up can still be controlled by the PORTD2 bit.

- **$\overline{\text{INT1}}$/AIN0, Bit 1**

INT1, External Interrupt source 1: The PD1 pin can serve as an external interrupt source to the MCU.

AIN0, Analog Comparator Positive input. This pin is directly connected to the positive input of the Analog Comparator.

- **$\overline{\text{INT0}}$/OC0B, Bit 0**

INT0, External Interrupt source 0: The PD0 pin can serve as an external interrupt source to the MCU.

OC0B, Output Compare Match B output: The PD0 pin can serve as an external output for the Timer/Counter0 Output Compare. The pin has to be configured as an output (DDD0 set “one”) to serve this function. The OC0B pin is also the output pin for the PWM mode timer function.

Table 11-10 and Table 11-11 relates the alternate functions of Port D to the overriding signals shown in Figure 11-5 on page 72.

Table 11-10. Overriding Signals for Alternate Functions PD7..PD4

Signal Name	PD7/T0/INT7/$\overline{\text{HBW}}$/$\overline{\text{CTS}}$	PD6/INT6/$\overline{\text{RTS}}$	PD5/XCK/PCINT12	PD4/INT5
PUOE	CTS	RTS	0	0
PUOV	PORTD7 • $\overline{\text{PUD}}$	0	0	0
DDOE	CTS	RTS	0	0
DDOV	0	1	0	0
PVOE	0	$\overline{\text{RTS}}$ OUTPUT ENABLE	XCK OUTPUT ENABLE	0
PVOV	0	$\overline{\text{RTS}}$ OUTPUT	XCK1 OUTPUT	0
DIEOE	INT7/$\overline{\text{CTS}}$ ENABLE	INT6 ENABLE	PCINT12 ENABLE	INT5 ENABLE
DIEOV	1	1	1	1
DI	T0 INPUT INT7 INPUT $\overline{\text{CTS}}$ INPUT	INT6 INPUT	XCK INPUT PCINT12 INPUT	INT5 INPUT
AIO	–	–	–	–

Table 11-11. Overriding Signals for Alternate Functions in PD3..PD0[1]

Signal Name	PD3/INT3/TXD1	PD2/INT2/RXD1/AIN1	PD1/INT1/AIN0	PD0/INT0/OC0B
PUOE	TXEN1	RXEN1	0	0
PUOV	0	PORTD2 • $\overline{\text{PUD}}$	0	0
DDOE	TXEN1	RXEN1	0	0
DDOV	1	0	0	0
PVOE	TXEN1	0	0	OC0B ENABLE
PVOV	TXD1	0	0	OC0B
DIEOE	INT3 ENABLE	INT2 ENABLE AIN1 ENABLE	INT1 ENABLE AIN0 ENABLE	INT0 ENABLE
DIEOV	1	AIN1 ENABLE	AIN0 ENABLE	1
DI	INT3 INPUT	INT2 INPUT/RXD1	INT1 INPUT	INT0 INPUT
AIO	–	AIN1 INPUT	AIN0 INPUT	–

Note: 1. When enabled, the 2-wire Serial Interface enables Slew-Rate controls on the output pins PD0 and PD1. This is not shown in this table. In addition, spike filters are connected between the AIO outputs shown in the port figure.

11.4 Register Description for I/O-Ports

11.4.1 Port B Data Register – PORTB

Bit	7	6	5	4	3	2	1	0	
	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	PORTB
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

11.4.2 Port B Data Direction Register – DDRB

Bit	7	6	5	4	3	2	1	0	
	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	DDRB
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

11.4.3 Port B Input Pins Address – PINB

Bit	7	6	5	4	3	2	1	0	
	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	PINB
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	

11.4.4 Port C Data Register – PORTC

Bit	7	6	5	4	3	2	1	0	
	PORTC7	PORTC6	PORTC5	PORTC4	-	PORTC2	PORTC1	PORTC0	PORTC
Read/Write	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

11.4.5 Port C Data Direction Register – DDRC

Bit	7	6	5	4	3	2	1	0	
	DDC7	DDC6	DDC5	DDC4	-	DDC2	DDC1	DDC0	DDRC
Read/Write	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

11.4.6 Port C Input Pins Address – PINC

Bit	7	6	5	4	3	2	1	0	
	PINC7	PINC6	PINC5	PINC4	-	PINC2	PINC1	PINC0	PINC
Read/Write	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	
Initial Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	

11.4.7 Port D Data Register – PORTD

Bit	7	6	5	4	3	2	1	0	
	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	PORTD
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

11.4.8 Port D Data Direction Register – DDRD

Bit	7	6	5	4	3	2	1	0	
	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	DDRD
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

11.4.9 Port D Input Pins Address – PIND

Bit	7	6	5	4	3	2	1	0	
	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	PIND
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	